

ABSTRACT

The technology of the present invention pertains to an apparatus and method for implementing a hardware-based performance monitoring mechanism for use in analyzing the behavior of a program module. The apparatus includes probe logic hardware that monitors the program's behavior in executing memory reference instructions. The probe logic hardware generates several probe signals which are transmitted to a performance monitor circuit when certain events occur. In an embodiment of the present invention, these events can be TLB or cache misses. The performance monitor circuit affixes a time stamp to the probe data and stores the time-stamped probe data in a temporary memory device until the data is stored in a magnetic storage device.

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